AMENDMENTS TO THE CLAIMS

1. (Currently amended) A pixel sensor cell comprising:

a pinned photodiode formed in a ~~an~~ Pwell that is formed in an N-type semiconductor substrate;

a depletion mode transfer transistor placed between the pinned photodiode and an output node;

a reset transistor coupled between a high voltage rail V_{dd} and the output node; and

an output transistor, the gate of the output transistor being coupled to the output node.

2. (previously presented) The pixel sensor cell of Claim 1 wherein said transfer transistor is a depletion mode MOSFET.

3. (previously presented) The pixel sensor cell of Claim 1, wherein the output node is the source of the transfer transistor and said pinned photodiode is the drain of said transfer transistor.

4. (previously presented) The pixel sensor cell of Claim 2, further including a negative voltage generator that generates a negative voltage sufficient to turn off said depletion mode transfer transistor.

5. (previously presented) The pixel sensor cell of Claim 2, wherein said depletion mode transfer transistor has a threshold voltage near V_{dd}.

6. (previously presented) The pixel sensor cell of Claim 2, wherein said depletion mode transfer transistor has a threshold voltage of substantially -0.9 volts or less.

7. (Currently amended) A CMOS image sensor comprising:

a plurality of active pixels arranged in rows and columns formed in an N-type semiconductor substrate, at least one of said active pixels comprising:

(a) a pinned photodiode;

(b) a depletion mode transfer transistor placed between the pinned photodiode and an output node, the transfer transistor being a depletion mode MOSFET; and

(c) a reset transistor coupled between a high voltage rail V_{dd} and the output node; and

(d) an output transistor, the gate of the output transistor being coupled to the output node.;

a negative charge pump for generating a negative voltage and formed in said N-type semiconductor substrate;

a processing circuit for receiving the output of said active pixels formed in said N-type semiconductor substrate; and

an I/O circuit formed in said N-type semiconductor substrate for outputting the output of said active pixels off of said CMOS image sensor.

8. (previously presented) The image sensor of Claim 7, wherein the output node is the source of the transfer transistor and said pinned photodiode is the drain of said transfer transistor.

9. (previously presented) The image sensor of Claim 7, wherein said depletion mode transfer transistor has a threshold voltage near V_{dd}.

10. (previously presented) The image sensor of Claim 7, wherein said depletion mode transfer transistor has a threshold voltage of substantially -0.9 or less volts.

11. (Currently amended) A CMOS image sensor comprising:

a plurality of active pixels arranged in rows and columns formed in an N-type semiconductor substrate, at least one of said active pixels comprising:

(a) a pinned photodiode;

(b) a depletion mode transfer transistor placed between the pinned photodiode and an output node; and

(c) a reset transistor coupled between a high voltage rail V_{dd} and the output node; and

(d) an output transistor, the gate of the output transistor being coupled to the output node.;

a negative charge pump for generating a negative voltage and formed in said N-type semiconductor substrate;

a processing circuit for receiving the output of said active pixels formed in said N-type semiconductor substrate; and

an I/O circuit formed in said N-type semiconductor substrate for outputting the output of said active pixels off of said CMOS image sensor.

12. (previously presented) The pixel sensor of Claim 11 wherein said transfer transistor is a depletion mode MOSFET.

13. (previously presented) The image sensor of Claim 11, wherein the output node is the source of the transfer transistor and said pinned photodiode is the drain of said transfer transistor.

14. (previously presented) The image sensor of Claim 12, wherein said depletion mode transfer transistor has a threshold voltage near Vdd.

15. (previously presented) The image sensor of Claim 12, wherein said depletion mode transfer transistor has a threshold voltage of substantially -0.9 or less volts.